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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/702,963	10/31/2000	Gary C. Hess	2	8994

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/702,963	HESS, GARY C.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the present Application filed 10/31/2000. Claims 1-38 are pending and are hereby presented for examination.

Specification

2. The abstract of the disclosure is objected to because of minor informalities. On line 3, the term "to inputs" should be deleted from the Abstract, because it does not describe clearly the claimed invention. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claim 4 is objected to because of the following informalities:

Claim 4, line 1, recites the term "understands", which should be changed as to better describe the function of the tester with respect to system requirements.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-29, 31-35, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Garner et al. (US 5745501), ISSUED: April 28, 1998, FILED: March 26, 1997.

Regarding independent Claim 1, Garner discloses a method of generating test script read by automated test equipment ATE, Figure 5, comprising:

Inputting stimulus values (202) and a model (208) of a computer component object, integrated circuit (10), into a generator coupled to the output of module patterns (212), Figure 5.

Converting stimulus values (202) and the model (208) into test script using translation block (214) to produce the integrated circuit patterns at 218, which are applied to the translator (224), which produces test vectors 226 and the strobes necessary to collect data produced by the integrated circuit under test (10).

Regarding independent Claims 11, 19, Garner discloses a method and apparatus of inputting data into a test generator, Figure 5, comprising:

First input for inputting system requirements (202) and second input for inputting testing requirements (208) into the test generator, which is coupled to the output of module patterns (212), Figure 5, wherein the system requirements are input from a different source (202) from the testing requirements (208).

And a converter that converts the testing requirements (208) and system requirements (202) into test script, using translation block (214) to produce the integrated circuit patterns at 218, which are applied to the translator (224), which produces test vectors 226 and the strobes necessary to collect data produced by the integrated circuit under test (10).

Regarding Claims 27 and 35, Garner discloses a method and apparatus to test response of a computer component integrated circuit (10), comprising:

Providing a model (208) of the computer component object, integrated circuit (10).

Providing stimulus values (202) to be applied to the computer component object, integrated circuit (10).

Converting stimulus values (202) and the model (208) into test script using translation block (214) to produce the integrated circuit patterns at 218, which are applied to the translator (224), which produces test vectors 226 and the strobes necessary to collect data produced by the integrated circuit under test (10).

Regarding Claims 2, 3, 12, 20, 33, Garner discloses a tester input for inputting the stimulus values (202), Step 128 of the method 120, accordingly: "the functionality of an integrated circuit 10 is verified by placing the integrated circuit in a tester, applying integrated circuit test patterns to the integrated circuit using the tester, obtaining output from the integrated circuit 10 using the tester, and checking the output against expected patterns contained in the integrated circuit test patterns".

Regarding Claim 4, Garner discloses tester system requirements according to integrated circuit data at block 216, and wherein the stimulus values (202) are prepared in response to the system requirements.

Regarding Claims 5, 13, 21, 29, Garner discloses modeler (208) that designs a model, based on the module drive patterns, which are applied to module models at block 208 and module expected patterns are produced, as represented at block 210.

Regarding Claims 6, 13, Garner discloses converting the module test stimuli (202) and the module models (208) into test script using translation block (214) to

produce the integrated circuit patterns at 218, which are applied to the translator (224), which produces test vectors 226 and the strobes necessary to collect data produced by the integrated circuit under test.

Regarding Claims 7, Garner discloses modeler (208), which designs the model of the computer component object integrated circuit (10) in response to testing requirements.

Regarding Claims 8, 14, 16, 22, 24, 28, Garner discloses that the test script (test vectors 226) is executed by the tester.

Regarding Claims 9, 10, 17, 18, 25, 26, Garner discloses the results, at block 230, from the actual test of the integrated circuit are verified against the expected results of the test vectors and stored in the tester.

Regarding Claims 15, 23, Garner discloses generating test script in response to the system requirements (202) and the testing requirements (208).

Regarding Claims 31, 32, 37, 38, Garner discloses a computer component object such as integrated circuit (10).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garner et al. (US 5745501), ISSUED: April 28, 1998, FILED: March 26, 1997.

Regarding Claims 30, 36, Garner does not explicitly disclose a graphical user interface (GUI) as a computer component object behavior. However, it is well know in the art to use (GUI) as component object behavior in the automatic test systems. Furthermore, (Figure1, Garner) illustrates a prior art modular integrated circuit, which can be integrated with a (GUI). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to integrate a (GUI) with Garner's prior art modular integrated circuit, since the integrated circuit 10 includes a CPU with associated peripheral devices that are compatible with GUI functionality. A person skilled in the art would have been motivated to use a GUI for providing visual display of testing.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov
Date: 8 December 2004
Office Action: Non-Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100